REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 2-6, 13-15, and 18 are active in the present application. Claims 2 and 3 are amended, and Claim 18 is added by the present amendment. Claims 7-12, 16, and 17 are withdrawn in response to a previous Restriction Requirement.

Amendments to the claims and the new claim find support in the application as originally filed at least at Figures 2 and 10, at page 12, lines 18-23, and at page 20, line 22 to page 21, line 2. Thus, no new matter is added.

In the outstanding Office Action, Claims 2, 3, 6, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent 5,270,230 to Sakurai in view of U.S. Publication 2001/0040255 to Tanaka; Claims 4 and 13 were rejected under 35 U.S.C. § 103(a) as unpatentable over Sakurai in view of Tanaka and Akiyama et al., "Effects of Shorted...," hereinafter "Akiyama"); Claims 5 and 14 were rejected under 35 U.S.C. § 103(a) as unpatentable over Sakurai in view of Tanaka and U.S. Patent 6,798,040 to Reznik; Claims 2, 3, 6, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Publication 2002/0048855 to Matsudai et al. (herein "Matsudai") in view of Tanaka; Claims 4 and 13 were rejected under 35 U.S.C. § 103(a) as unpatentable over Matsudai in view of Tanaka and Akiyama; Claims 5 and 14 were rejected under 35 U.S.C. § 103(a) as unpatentable over Matsudai in view of Tanaka and Reznik; Claims 1-3, 6, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Tanaka in view of Sakurai; Claims 4 and 13 were rejected under 35 U.S.C. § 103(a) as unpatentable over Tanaka in view of Sakurai and Akiyama; and Claims 5 and 14 were rejected under 35 U.S.C. § 103(a) as unpatentable over Matsudai in view of Tanaka and Reznik.

Applicants respectfully traverse the rejections of Claims 2-6 and 12-15 with respect to Sakurai, Tanaka, Akiyama, Reznik, and/or Matsudai, with respect to amended independent Claims 2 and 3.

Claim 2 is directed to an insulated gate bipolar transistor that includes, in part, a semiconductor substrate of a first conductivity type including a first main surface and a second main surface, an insulated gate transistor, a first main electrode formed on the first main surface and in contact with a base region of the insulated gate transistor at the first main surface, and a first semiconductor layer of the first conductivity type formed on the second main surface of the semiconductor substrate, facing the insulated gate transistor, and vertically aligned with a region of the first main electrode in contact with the base region. Claim 3 includes similar features.

In a non-limiting embodiment, Applicants' Figure 2 shows an example of an insulated gate bipolar transistor that includes a semiconductor substrate 1 and an insulated gate transistor formed in a region of the semiconductor substrate on a side of the semiconductor substrate that includes the first main surface. In particular, the insulated gate transistor also includes a first main electrode 7 in contact with a base region 2. In addition, a first semiconductor layer 8 is formed on the second main surface 1S2 facing the insulated gate transistor and vertically aligned with the region of the first main electrode that is in contact with the base region.

Applicants respectfully submit that the combined disclosures of Sakurai, Tanaka, Reznik, Matsudai, and Akiyama, whether taken individually or in combination, fail to teach or suggest each of the features of the amended independent claims. For example, none of the references teach or suggest a first semiconductor layer formed on a second main surface of the semiconductor substrate that faces the insulated gate transistor and is vertically aligned with a region of the first main electrode in contact with the base region.

First, Applicants respectfully note that Matsudai and Reznik each fail to teach or suggest first and second semiconductor layers formed on a second main surface of a semiconductor substrate. Accordingly, Matsudai and Reznik also fail to teach or suggest a first semiconductor layer that is vertically aligned with a portion of the insulated gate transistor.

Akiyama shows an insulated gate bipolar transistor having P^+ and N^+ collector shorting regions (e.g., first and second semiconductor layers) arranged along a lower electrode (e.g., second main electrode).[1] However, Akiyama does not indicate any alignment of the P^+ and N^+ shorting regions with respect to any portion of the insulated gate bipolar transistor.

Tanaka shows various insulated gate bipolar transistor embodiments in Figures 4-12 having P^+ and N^+ regions 2b and 12, respectively (e.g., second and first semiconductor layers). However, Tanaka also does not indicate any particular alignment of these P^+ and N^+ regions with respect to any portions of the insulated gate transistor.

In addition, Sakurai indicates examples of insulated gate bipolar transistors in Figures 1-3, 5A, 5B, and 6. However, although various embodiments of Sakurai indicate structures arranged on a second surface of the semiconductor substrate, Sakurai also fails to teach or suggest any alignment of the structures on the second surface with any feature of the insulated gate transistor on the first main surface.

Accordingly, Applicants respectfully submit that none of the references in the outstanding Office Action, when taken individually or in combination, teach or suggest "a first semiconductor layer of said first conductivity type formed on said second main surface of said semiconductor substrate, facing said insulated gate transistor, and vertically aligned

[1] Akiyama at Figure 1A.

with a region of the first main electrode in contact with said base region," as recited in independent Claims 2 and 3.

Accordingly, Applicants respectfully submit that independent Claims 2 and 3, and claims depending therefrom, patentably define over Sakurai, Tanaka, Reznik, Matsudai, and Akiyama.

Thus, it is respectfully requested the rejections of Claims 2-6 and 12-15, with respect to Sakurai, Tanaka, Reznik, Matsudai, and Akiyama, be withdrawn.

Further, new Claim 18 is directed to an insulated gate bipolar transistor with features similar to those recited in Claims 2 and 3. However, in new Claim 18, the second semiconductor layer of the second conductivity type is vertically aligned with a region of the first main electrode, for example, as shown in the non-limiting embodiment of Figure 10. Thus, Applicants respectfully submit that independent Claim 18 is also allowable.

Therefore, it is respectfully submitted that independent Claims 2, 3, and 18, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment, this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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